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09/750,093	12/29/2000	Michael Cornaby	2207/9806	6385

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EXAMINER	
MEONSKE, TONIA L	
ART UNIT	**PAPER NUMBER**
2183	5

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/750,093	Applicant(s) CORNABY ET AL.	
	Examiner Tonia L Meonske	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 is objected to for failing to comply with 35 U.S.C. 112. Claim 6 recites the limitation "the microinstruction core unit" in line 6. There is insufficient antecedent basis for this limitation in the claim. Please change the limitation to read "the microprocessor core unit". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Goss et al., US Patent 3,909,797.

6. Referring to claim 1, Goss et al. have taught a microinstruction sequencer including a microinstruction sequencer stack comprising an array of memory cells (Figure 2, element 60, including elements 62, 64, 66, and 68) and control logic (Figure 2), said microinstruction sequencer stack coupled to receive data and control values from one of a microinstruction

sequencing logic (Figure 2, elements 54, 56, and 58) and a microprocessor core unit (The entire system in Figure 1 is a microprocessor core unit.).

7. Referring to claim 2, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microprocessor core unit is an execution unit (Figure 1).

8. Referring to claim 3, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microprocessor core unit is a retire unit (Abstract, column 2, lines 39-44, In order for the instructions in the subroutine to be completed, there must inherently be unit that performs the completing.).

9. Referring to claim 4, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. generate a value of a microinstruction address (Figure 2, Element 56 contains the generated microinstruction address.);

b. add an intermediary value to the value of the microinstruction address to yield an incremented value (Figure 2, element 58);

c. send a control value to the microinstruction sequencer stack, said control value to cause the incremented value to be pushed onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.); and

d. push the incremented value onto the microinstruction sequencer stack (Abstract, Column 7, lines 60-64).

10. Referring to claim 5, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to:

i. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

ii. send the popped value to a microinstruction address multiplexer (Figure 2, element 54).

11. Referring to claim 6, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to:

a. send a control value to the microinstruction sequencer stack, said control value to:

i. cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62); and

ii. send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52), said immediate logic to pass the value to the microinstruction core unit (Figure 2, Element 52 passes the value to the core unit.).

12. Referring to claim 7, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to push a value in an immediate field of a microinstruction onto the microinstruction sequencer stack (Figure 2, The output of Element 58 is the control value that causes the incremented value to be pushed onto the stack.).

13. Referring to claim 8, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to return to a reset state (Inherent, Must be able to initialize the system to a known state.).

14. Referring to claim 9, Goss et al. have taught the microinstruction sequencer of claim 1, wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 send control values to the stack.), said control value to cause the microinstruction sequencer stack to pop a value (abstract, column 8, lines 49-62) and send the popped value to an immediate logic (Figure 2, elements 54, 56, 50, and 52).

15. Referring to claim 10, Goss et al. have taught the microinstruction sequencer of claim 1, as described above, and wherein the microinstruction sequencing logic includes logic to send a control value to the microinstruction sequencer stack (Figure 2, Element 58 sends the control value to the stack.), said control value to cause the microinstruction sequencer stack to send a value at the top of the microinstruction sequencer stack to an immediate logic (abstract, column 8, lines 49-62, Figure 2, elements 54, 56, 50, and 52).

16. Claim 11 does not recite limitations above the claimed invention set forth in claims 1 and 2 and is therefore rejected for the same reasons set forth in the rejection of claims 1 and 2 above.

17. Referring to claim 12, Goss et al. have taught the microinstruction sequencer of claim 11, as described above, and wherein the microprocessor execution unit includes logic to:

a. read a register value (Figure 2, The value from the register, element 56, is read out and sent to the stack.); and

b. communicate the register value to the microinstruction sequencer stack (The value from the register, element 56, is read out and sent to the stack.).

18. Referring to claim 13, Goss et al. have taught a microprocessor including a microinstruction sequencer comprising:

a. an array of memory cells dedicated to said microinstruction sequencer (Figure 2, elements 62, 64, 66, and 68);

b. an address multiplexer coupled to said array of memory cells (Figure 2, element 54);

c. sequencing logic coupled to said address multiplexer and to said array of memory cells (Figure 2, elements 56, 50, 52, and 58); and

d. a microprocessor core unit coupled to said array of memory cells (The entire system in Figure 1 is a microprocessor core unit.).

19. Referring to claim 14, Goss et al. have taught the microinstruction sequencer of claim 13, wherein the microprocessor core unit is an execution unit (Figure 1).

20. Referring to claim 15, Goss et al. have taught the microinstruction sequencer of claim 13, as described above, and wherein the microprocessor core unit is a retire unit (Abstract, column 2, lines 39-44, In order for the instructions in the subroutine to be completed, there must inherently be unit that performs the completing.).

21. Referring to claim 16, Goss et al. have taught a method of directing the sequence of execution of microinstructions during a call to and return from a subroutine (abstract), comprising:

a. receiving a microinstruction at a microinstruction sequencing logic (abstract, Figure 1, element 18);

b. pushing a value in a field of the microinstruction onto a microinstruction sequencer stack, the value is a return address of the subroutine (abstract, Column 7, lines 60-64);

c. executing the subroutine (abstract, column 7, line 64-column 8, line 2);

d. popping the value from the microinstruction sequencer stack to a microinstruction address multiplexer (abstract, abstract, column 8, lines 49-62 Figure 2, element 54); and

e. returning to the return address of the subroutine by sequencing the value from the address multiplexer to a microinstruction sequencer (abstract, Figure 2, The value is sequenced to elements 56, 50 and 52.).

22. Referring to claim 17, Goss et al have taught the method of claim 16, as described above, and wherein the value is the address of the call of the subroutine plus one (column 8, lines 42-47).

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

24. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

25. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER